Claims

What is claimed is:

[c1] An apparatus for modeling an anti-resonance circuit of a microprocessor, comprising:

a load model that simulates the anti-resonance circuit;

a transistor that simulates at least one high frequency capacitor, wherein the transistor is connected in parallel with the load model; and

a capacitor that simulates an intrinsic capacitance of a section of the microprocessor, wherein the capacitor is connected in parallel with the load model.

[c2] The apparatus of claim 1, wherein the load model simulates the anti-resonance circuit with a resistor.

[c3] The apparatus of claim 2, wherein the resistor is a voltage controlled resistor.

[c4] The apparatus of claim 1, wherein the load model simulates the anti-resonance circuit in synchronization with a clock cycle.

[c5] The apparatus of claim 4, wherein the clock cycle is generated by a central processing unit clock.

[c6] The apparatus of claim 4, wherein the load model begins to simulate the anti-resonance circuit on a leading edge of the clock cycle.

[c7] An apparatus for modeling an anti-resonance circuit of a microprocessor, comprising:

means for simulating an anti-resonance circuit; and

means for synchronizing the means for simulating an anti-resonance circuit with a clock signal.

[c8] A method for modeling an anti-resonance circuit of a microprocessor, comprising:

modeling a load to generate a simulation of an anti-resonance circuit;

simulating at least one high frequency capacitor in parallel with the load model; and

simulating a section of the microprocessor's intrinsic capacitance in parallel with the load model.

[c9] The method of claim 8, wherein the load is modeled with a resistor.

[c10] The method of claim 9, wherein the resistor is a voltage controlled resistor.

[c11] The method of claim 8, wherein the simulation of the anti-resonance circuit is synchronized with a clock cycle.

[c12] The method of claim 11, wherein the clock cycle is generated by a central processing unit clock.

[c13] The method of claim 11, wherein the simulation of the anti-resonance circuit begins on the leading edge of the clock cycle.